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12EC027

M. Tech. Degree Examination, Dec.2014/Jan.2015
Design of VLSI Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Draw and explain the 16 bit carry look ahead adder. Write down the expression for critical path delay. **(08 Marks)**

b. Explain array funnel shifter, with a neat diagram. **(06 Marks)**

c. Explain the concept of hierarchy in VLSI designs. **(06 Marks)**

2 a. With the help of a neat diagram, explain unsigned magnitude comparator. **(08 Marks)**

b. Explain the terms regularity, modularity and locality with one example for each. What are the advantages of this approach? **(12 Marks)**

3 a. Obtain the schematic of 8 : 1 multiplexer using 4 : 1 multiplexer and 2 : 1 multiplexer. **(08 Marks)**

b. Discuss the various components which accounts for nonrecurring engineering costs (NREC). **(07 Marks)**

c. With necessary diagram, explain the simple Manchester adder with carry bypass. **(05 Marks)**

4 a. With the help of a 6T RAM cell, explain memory read and write operation and draw corresponding graphs. **(12 Marks)**

b. Draw and explain 4 × 4 CAM array. Give an application of CAM array and explain the same. **(08 Marks)**

5 a. Design a BILBO structure for linear feedback shift register implementing the function $f = 1 + x + x^3$. Draw the schematic and explain. **(12 Marks)**

b. Explain controllability, observability and fault coverage. **(08 Marks)**

6 a. Design and implement 3 – bit synchronous arbitrary counter to generate the sequence 0, 1, 2, 3, 6, 5, 7 and repeat using toggle flip flops. **(10 Marks)**

b. What are error – correcting codes and gray codes? Explain with examples. **(10 Marks)**

7 a. What are serial and parallel divisions? Divide 13 by 34 using serial division method and divide 11 by 2 using parallel method. **(12 Marks)**

b. Explain bitrine conditioning in SRAM with the help of a diagram. **(04 Marks)**

c. With the help of a diagram, explain column circuitry in a DRAM cell. **(04 Marks)**

8 a. With the help of a neat diagram, explain boundary scan architectures. **(10 Marks)**

b. List the ideal properties of packaging. **(05 Marks)**

c. Explain the following global clock distribution :

i) Grids

ii) H – trees. **(05 Marks)**

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